M.Sc. Examination 2018
Semester-II
Computer Science
Course : MCSC-24
(Advanced Architecture)

Time : 3 Hours **Full Marks : 40**

Questions are of value as indicated in the margin

Answer Question No.**1** and **any three** from the rest

1. Answer **any five** questions : 2×5=10
   a) Discuss the differences between UMA an NUMA architecture?
   b) How code morphing software ensures *binary compatibility*?
   c) What are the problems of MIPS rating system?
   d) Discuss the differences between RISC and CICS architecture.
   e) State and explain Amdah's Law.
   f) Write down the addressing modes supported by a MIPS processor.
   g) How can we eliminate structural hazards?
2. How can we measure a processor's performance using different types of benchmark? Let us assume that you have profiled your code and the instruction mix is detailed in the following table. We now want to build and optimizing compiler for the CPU. The compiler discards 40% of the ALU instructions and 50% of the Load instructions although it cannot reduce stores, or branches. Assuming a 20-ns clock cycle time (or the Load instructions although it cannot reduce stores, or branches. Assuming a 20-ns clock cycle time (or a 50-MHz clock), what is the MIPS rating for the optimized code versus the unoptimized code? Does the MIPS rating agree with ranking execution time?

Operation	Frequency	CPT
ALU Operations	33%	1
Loads	31%	2
Stores	12%	2
Branches	24%	2

3+(5+2)=10

3. Discuss *Register Indirect* and *Based-Index* addressing modes. Discuss the role of pipeline registers? How many pipeline registers do ou need for a typical MIPS processor. Assume that a multiple cycle RiSC implementation has a 10 ns clock cycle, loads take 5 clok cycles, account for 30% of the instruction , store take 4 clock cycles, account for 25% of the instruction and all other instructions take 4 cycles. If we apply pipelining the machine adds 1 ns to the clock cycle (due to the pipelined registers), how much speedup in instruction execution rate do we get from pipelining with multi clock cycle and single clock cycle approach? 3+(2+1)+4=10
4. Discuss the differences between Synchronous and Asynhronous pipeline. Develop a pipelined fixed point multiplier. Identify the data hazards present in the following code then show how we can avoid these hazards by applying *Forwaring and bypassing technique*?

P.T.O.

lw $1, 4 ($2)
Sub $4, $1, $5
and $6, $1, $7
or $8, $1, $9
xor $4, $1, $5 2+4+4=10

5. Consider following code snippet in C and write the MIPS equivalent code. Using the MIPS code and latency table, show how the compiler can increase the ILP by using loop unrolling with scheduling technique. Assume that loop unrolling factor is 4

   For (i = 1000;i >0 : i=i–1)

   x[i] = x [i] + 8

Source In (*independent*)	User In (*dependent*)	Latency
FP	FP ALU OP	3
FP ALU OP	Store Double	2
Load Double	FP ALU OP	1
Load Double	Store Double	0

   What are the limitations of scalar pipelined processor? 1.5+6+2.5=10

6. What are the drawbacks of VLIW processors? Show that the performance of super pipelined-superacalar processor is better than a superscalar processor? Why dynamic instruction Scheduling is needed? Describe Dynamically Scheduled Speculative pipeline. 2.5+2.5+2.5+2.5=10

7. Suppose we have a superscalar MIPS processor with following specification.

Functional Units (FU	Number of FUs	EX cycle
Integer	1	1
Floating point multiply	2	10
Floating point Add	1	2
Floating point divide	1	40
Number of Registers		31

   The following code is run on the above mentioned MIPS processor.

```
L.D      F6, 34 (R2)
L.D      F2, 45 (R3)
MUL.D    F0, F2, F4
SUB.D    F8, F6, F2
DIV. D   F10, F0, F6
ADD.D    F6, F8, F2
```

   Identify various dependencies exist between these instructions and draw a data dependency graph. Apply *Scoreboard* technique on the above stated code. Assume that this scoreboard consists of three parts: the instruction status, the functional unit status, and the register result status. What are limitations of this technique? 2+7+1=10

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