B.Sc.(Honours)Examination, 2018

Semester–V

Physics (Honours)

Course: BPC-52

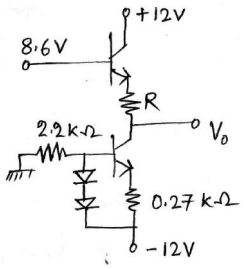
(Electronics-II)

Time: Three Hours **Full Marks: 40**

Questions are of value as indicated in the margin.

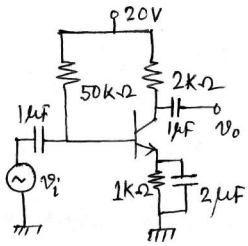
Answer ***any four*** questions.

1. a) What do you mean by bias stability of a transistor? Determine the emitter current and stability factor of a typical fixed bias circuit.
   b) Calculate the value of R for which V_0 becomes zero in the given circuit. (Assume β is very large)



2+4+4

2. a) Calculate the current gain (A_i) and voltage gain (A_v) of the amplifier shown below. Take $h_{ie} = 560\Omega,\ h_{fe} = 100.$



what will happen in A_i and A_v if the bypass capacitor 2μF is withdrawn.
   b) Show how the gain of an RC coupled amplifier varies with frequency. Explain it. 3+3+4

3. a) The gain of an amplifier is 500. It is used in a negative feedback loop with feedback ratio of 0.01. If due to temperature or other causes the gain (without feedback) changes by 20%, what would be the corresponding change in gain with feedback. Also calculate the gain with feedback.
   b) Derive the expression for the frequency of oscillation and the condition of oscillation for a tuned-collector oscillator. 4+6

4. a) Find octal equivalent of a HEX number 5A3.
   b) In a code of base 5 the digits are 0, 1, 2, 3, 4. Find the equivalent of a number 312_{10} in this code.
   c) Draw the internal circuit diagram of a 2-input NAND gate and verify its truth table.
   d) Simplify the following expression to implement using only NAND gates:
   $f = \Pi M\left(1,5,7,12-15\right).$ 2+2+3+3

5. a) Design a Full-Adder circuit using only 7400 ICs.
   b) How can you design a JK Flip-Flop using SR?

P.T.O.

c) Design a synchronous counter with the following sequence of states

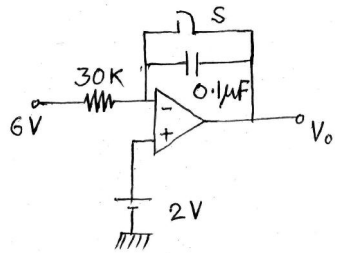
A	B	C
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0

3+3+4

6. a) Explain (i) virtual ground and (ii) CMRR with respect to an OP-AMP.
   b) Calculate the output voltage of an OP-AMP if

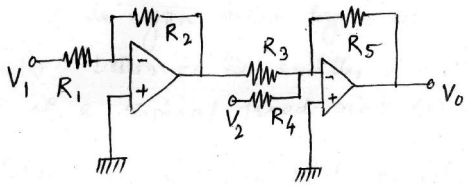
   $v_{i1} = 500\mu V$, $v_{i2} = 300\mu V$, $A_d = 10^3$ and CMRR $= 10^4$.

   c) Draw the circuit diagram of a practical integrator using OP-AMP. In the following diagram the switch 'S' is initially closed. Draw V_0 for 20 ms after S is opened.



2+3+5

7. a) Show the condition for which $V_0 = V_1 - V_2$ is obtained in the given circuit



   b) Draw the circuit diagram of a logarithmic amplifier using OP-AMP. Derive its output voltage.
   c) How can you obtain astable multivibration from a circuit designed using OP-AMP. 4+3+3

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