M.Sc. Semester-II Examination 2017
Computer Science
Course : MCSC-24
(Advance Computer Architecture)

Time : 3 Hours **Full Marks : 40**

Questions are of value as indicated in the margin

Answer question number **1** and **any three** from the rest

1. Answer following questions (**any five**) : 5×2=10
   (a) What is meant by '*Binary compatibility*'? Why it is important during processor upgradation?
   (b) Discuss the limitations of scalar processor.
   (c) What are the advantages of *out-of-order* execution of a set of instructions over *in-order* execution?
   (d) What are the drawbacks of synthetic benchmark?
   (e) Discuss '*inclusion*' and '*coherence*' properties of the memory hierarchy system.
   (f) What is '*control dependence*'?
   (g) Compare VLIW and super scalar processor.
2. Discuss different types of parallelism which can be used to improve a processor's performance.

   Consider two different implementations, M1 and M2, of the same instruction set, There are three classes of instructions (A, B, and C) in the instruction set. M1 has a clock rate of 80 MHz and M2 has a clock rate of 100 MHz. The average number of cycles for each instruction class and their frequencies (for a typical program) are as follows:

Instruction Class	Machine M1- Cycles/Instruction Class	Machine M2- Cycles/Instruction Class	Frequency
A	1	2	60%
B	2	3	30%
C	4	4	10%

   Which machine has a smaller MIPS rating? Which individual instruction class CPI do you need to change, and by how much? How this machine is having the same or better performance as the machine with the higher MIPS rating (you can only change the CPI for one of the instruction classes on the slower machine)? 4+3+3=10
3. Discuss "Indexed" and "Relative" addressing mode.

   Suppose you are trying to implement a four stage pipe line processor. These stages are:

   (i) Instruction Fetch (ii) Instruction decode (iii) Execution (iv) Memory and Write Back

   Show the implementation and operations of the fourth stage (i.e. Memory and Write Back). Discuss advantages (if any) and disadvantages (if any) of your processor over conventional five stage MIPS processor. (1.5+1.5)+(2+3)+2=10
4. Distinguish between instruction pipeline and arithmetic pipeline. Develop a pipelined floating point adder. Compute the speed up of super pipelined-superscalar processor w.r.t. scalar processor, superscalar, and super pipelined processor. 2+3.5+(1.5+1.5+1.5)=10

P.T.O.

5. Discuss software pipelining approach with following example. Assume that the loop unrolling factor is 3.

```
Loop:   L.D       F0,0(R1); F0=array element
        ADD.D     F4,F0,F2; add scalar in F2
        S.D       F4,0(R1): store result
        DADDUI    R1, R1,#-8;decrement pointer
        BNE       R1, R2,loop; branch if R1!=R2
```

   Compare software pipelining and loop unrolling approach. Discuss the disadvantages of software pipelining. 6+3+1=10

6. Suppose we have a superscalar MIPS processor with following specification.

Functional Units (FU)	# of FUs	FX cycle
Integer	2	1
Floating point multiply	1	10
Floating point Add	2	2
Floating point divide	1	40

Number of Register	31

   The following code is run on the above mentioned MIPS processor.

```
Loop:   L.D       F2,0(R1)
        ADD.D     F6,F2,F4
        MULT.D    F8,F6,F0
        L.D       F10,8(R1)
        ADD.D     F12,F10,F4
        MULT.D    F14,F12,F0
        SUBI      R1,R1,#16
        BNEZ      R1, Loop
```

   Identify various dependences between these instructions and draw a data dependency graph. Apply 'Scoreboard' technique on the above stated code. Assume that this scoreboard consists of three parts: the instruction status, the functional unit status, and the register result status. 3+7=10

7. Discuss different types of RAM and their advantages and disadvantages. Discuss '*set associative*' technique to map a main memory block into a cache line. Discuss merits and demerits of this technique. 4.5+3.5+2=10

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