M.Sc. Examination, 2019
Semester-II
Computer Science
Course : MCSC-24
(Advanced Architecture)

Time : 3 Hours **Full Marks : 40**

Questions are of value as indicated in the margin

Answer Question No.**1** and **any four** from the rest.

1. Answer **any four** from the followings. 4×2=8
   a) What are write through and write back protocols related to cache memory?
   b) What do you understand by cache coherence?
   c) Explain property of locality of reference.
   d) Explain the terms miss ratio and miss penalty.
   e) What is memory interleaving? Why it is so useful.
   f) What is the purpose of 1/O Module?

2. a) What do you mean by pipelining of a system? Define the term speedup ratio?
   b) Prove that for a pipelining system of k segments the maximum speed up can be achieved is k.
   c) Consider a 4(k = 4) segment pipeline with a clock cycle time t_p = 20ns and the pipeline system executes n tasks in sequence. Assume each task requires one clock cycle to be completed. Calculate the speed up ratio for n = 40, 50,60,100 *and* 150. Comment on the obtained result. (0.5+0.5)+3+(1.5+2.5)=8

3. a) Why the cache memory is so important? How the performance of the cache is measured?
   b) Consider a cache consisting of 128 blocks 16 words each for a total of 2k words. The main memory has 4k blocks of 16 words each.
   With the help of above ex ample explain the Direct Mapping, Associative Mapping and Set-associative mapping for a cache. Discuss the advantages and disadvantages of above cache mapping schemes. Show that the Direct mapping and Associative mapping schemes are the limiting cases of the Set-Associative Mapping. (1+2)+(3+1+1)=8

4. a) State and Explain Amdhal's law for multiprocessor system. Give its graphical representation. Explain why it is difficult to achieve Linear Speed-up in a multiprocessor system? Explain the term Super-linear speedup.
   b) Consider a multiprocessor system having number of processors p=16 and consider an application whose parallelizable part f is 70%.
   i) Calculate the improvement in performance using Amdahl's law.
   ii) Two applications have parallelizable part f is 80% and 90%. Calculate the improvement in performance (speed up) using Amdhal's law for p = 32 and p = 64 for both the cases.
   iii) Comment on obtained results. (1.5+1+0.5+0.5)+1+3+0.5)=8

5. a) What do you mean by data stream (DS) and instruction stream(IS)? According to Flynn how the computers are classified depending upon numbers of DS and IS.
   b) Discuss the operations of each these classes with the help of a schematic diatgram.

P.T.O.

c) How processors in SIMD computers communicate among themselves during computation. Write down various classes of SIMD computers. (1+1)+4+(1+1)=8

6. a) When do page faults occur? Do you think that page fault is an error?

b) In virtual memory system the main memory has the capacity of 4 pages, consider the following page reference string 0,2,1,6,4,0, 1,0,3,1,2,1 and calculate the page fault rate with the page replacement algorithms OPT, FIFO and LRU.

c) Consider a computer system having 8k address space and 4k memory space. How much is the width of virtual address and physical add ress. Explain with the help of memory page table how the virtual address is mapped to physical address. 1+3+(1+3)=8

7. a) Compare and constrast Programmed I/O and Interrupt-driven I/O.

b) Explain memory mapped I/O and I/O mapped I/O.

c) What is DMA? What is the function of DMA Controller. What do you mean by cycle stealing DMA? Explain. What is robust mode DMA? 2+2+(1+2+1)=8

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